APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Please insert the following paragraph at page 1, between lines 2 and 3:

This is a division of application Serial No. 09/031,981, filed February 26, 1998.

Paragraph beginning at page 2, lines 4-18:

Meanwhile, since the distribution of electromagnetic field around input/output [section] sections of electronic components, such as semiconductor devices, and the distribution of electromagnetic field around planar dielectric [line] lines generally differ, merely mounting electronic component onto the planar dielectric line causes the conversion loss to increase greatly. Further, if electronic components are only mounted onto one surface of the dialectic plate, no connection is made between the electro magnetic field on the back surface thereof and the electronic components [is not made], this point also leading to an increase in the conversion loss. Mounting electronic components onto both surfaces of the dielectric plate eliminates the latter problem; however, this results in a decrease in the yield, an increase in loss, and an increase in the material and mounting costs.

Paragraph beginning at page 3, line 22 to page 4, line 8:

An RF signal of the LSM mode, which propagated through the planar dielectric line as described above, is coupled to the line-conversation conductor pattern, is converted into a TE mode, and propagated through the slot line. The signal which propagated through this slot line is [input] inputted to the electronic components. Conversely, the signal [output] outputted from the electronic components propagates through the slot line in the TE mode, is converted into the LSM mode by the line-conversion conductor pattern, and propagates through the planar dielectric line.

Paragraph beginning at page 5, lines 17-20:

The above and further objects, aspects and novel features of the invention will become more apparent from the following detailed description when read in connection with the accompanying drawings. In the drawings, like references denote like elements and parts and accordingly each references may not be described in connection with each specific drawing in which it appears.

Paragraph beginning at page 7, lines 2-4:

The construction of a high-frequency amplifier according to a first embodiment of the present invention will be described with reference to Figs. 1A and 1B, [to] 2, 3, 4, 5 and 6.

Paragraph beginning at page 7, line 5 to page 8, line 12:

Figs. 1A an 1B are partial, exploded perspective views showing the construction of the high-frequency amplifier. Fig.1A is a perspective view of a lower conductor plate, with a groove 43 being formed in the top surface of the lower conductor plate. Fig. 1B shows a state in which a substrate 30 is placed on the top surface of the lower conductor plate shown in Fig. 1A. The substrate 30 is such that various conductor patterns are formed on the top and bottom surfaces of the conductor plate, with a slot-line-input-type FET (millimetric-wave GaAs FET) 50 being mounted onto the top surface of the circuit substrate 30. Reference numerals 14 and 24 each denote a slot on the top surface of the substrate 30. Formed by disposing two conductors at a fixed distance, and, as will be described later, form two planar dielectric lines together with the opposing slot on the bottom surface of the substrate 30. Reference numerals 12 and 13 each denote a slot line formed at the end portions of the two planar dielectric lines (see also Fig. 5). Reference numerals 10 and 11 denote line-conversion conductor patterns which connects the planar dielectric lines 14, 24 and the slot lines 12, 13 (see also Fig. 5). Reference numerals 31 and 32 each denote a coplanar line, which supplies a gate bias voltage and a drain bias voltage to an FET 50. These two coplanar lines 31 and 32 are provided with filters indicated by F, and the peripheral portion of the coplanar lines 31 and 32 covers, as an RF-GND (grounding conductor), the top surface of the circuit substrate 30, and in the other area of the bottom surface of the circuit substrate 30, an RF-GND is formed.

Paragraph beginning at page 11, lines 13-21:

Further, the top surface of the space 42 in [the figure] Fig. 3 and the electrode 21a form a parallel-plate waveguide, and the thickness t42 thereof is set so that the cut-off frequency with respect to the TE wave of the parallel-plate waveguide becomes sufficiently higher than the desired propagation frequency fb. As a result, a cut-off area with respect to the TE wave is formed in the portion indicated by 42a. In a similar manner, a cut-off area with respect to the TE wave is formed in each of the portions indicated by 42b, 43a, and 43b. Propagation areas with respect to the TE wave are indicated by 42c and 43c.

Paragraph beginning at page 12, lines 7-14:

As a result of forming the planar dielectric line as described above, it is possible to cause the electromagnetic-field energy of a high-frequency signal having a frequency equal to or higher than the critical frequency fda to be concentrated in the inside of the propagation area 23c and in the vicinity thereof and to cause the plane wave to propagate in the direction of the length (in the direction of the z axis) of the conductor plate 23. (Note the x, y and z directions indicated in Figs. 3 and 4).

Paragraph beginning at page 13, lines 3-5:

The planar dielectric line shown in the above is similarly constructed in the portion where a slot 14 shown in Fig. [1] 1B is formed.

Paragraph beginning at page 13, lines 6 to page 14, lines 9:

Fig. 5 is a view showing the conductor patterns of the main portion of the top surface of the circuit substrate 30. In Fig. 5, reference numerals 12 and 13 each denote a slot line, which is formed in each of the end portions of two planar dielectric line. Reference numerals 10 and 11 each denote a line-conversion conductor pattern, which is formed in the shape of a dipole antenna, as indicated by 10a, 10b, 11a, and 11b, respectively. [Another] Other shapes of the portions 10a , 10b, 11a and 11b are possible as long as the portions function as dipole antennas. The base portions of the line-conversion conductor patterns 10 and 11 form impedance matching sections R which are tapered moderately from the slot lines 12 and 13 toward the line- conversion conductor patterns 10 and 11

in order that the writing resistance of the line-conversation conductor patterns 10 and 11 is reduced to decrease the conversion loss. If the wavelength of the frequency in the used frequency band in each of the electrode patterns 10a, 10b, 11a, 11b and the impedance matching section R is denoted as λ, they have a length of nearly $\lambda/4$, and the width of the slot lines 12 and 13 is determined by the characteristics impedance of the designed line. [When] [assuming] Assuming that Z_1 is the input impedance of the line-conversation conductor patterns 10 and 11, Z_{in} is the input impedance of a portion 100, Z_{01} is the impedance of a portion [11] L_1 and Z_{02} is the impedance of a portion [12] L_2, it is preferable that the relation of these values [are] is given by the following equation:

Paragraph beginning at page 14 between lines 11-17:

For example, a characteristic impedance of 30 to 100 Ω can be realized at a width of 0.05 to 0.20 mm. As described above, the characteristics impedance of the planar dielectric line is 30 to 200 Ω, and the input/output impedance of the FET (millimetric-wave GaAs FET) 50 (see Fig. 1B) is usually 30 to 90 Ω; therefore, the three, including the planar dielectric line, the slot line, and the FET, easily obtain impedance matching.

Paragraph beginning at page 15, line 18 to page 17, line 7:

Fig. 6 is a view showing a state in which the FET 50 is mounted with respect to the state shown in Fig. 5. In Fig. 6, reference numerals 51 and 52 denote the source terminals of the FET 50, reference numeral 53 denotes a gate terminal, and reference numeral 54 denotes a drain terminal. The portions indicated by 55 and 56 are active areas. A field-effect transistor, such as an MES-FET (metal semiconductor FET) or a HEMT (high electron mobility transistor), is formed in each of the portions, and the source terminals 51 and 52, the gate terminal 53, and the drawing terminal 54 are extended out. Between the source terminals [51 and] 51, and the gate terminal 53 and the drain terminal 54, and between the gate terminal 53 and the drain terminal 54, and the source terminals [52 and] 52, a slot line is formed, as shown in the figure. The cross-hatched portion is a viahole formation portion, and each terminal is extended out to the back-surface side of the chip. If a gate bias voltage and a drain bias voltage are applied via the center conductors 33 and 34 of the coplanar lines 31 and 32, respectively, the FET 50 forms a complementary amplifying circuit. The arrows in the figure show the electric-field distribution of a signal which propagates through the slot lines

12 and 13. The signal of the LSM mode, which propagates from top to bottom in the figure through the planar dielectric line including the slot indicated by 14 in the figure, is converted into a mode (TE mode) of the slot line via the line-conversion conductor pattern 10, and this TE mode signal propagates through the slot line 12 and is applied, as a voltage signal, between the source and the gate of the FET 50. And the voltage signal between the source and the drain propagates through the slot line 13 again in the TE mode, and further, is converted into an LSM-mode signal via the line-conversion conductor pattern 11. This signal is propagated through the planar dielectric line, including the slot indicated by 24, in the downward direction in the figure.

Paragraph beginning at page 19, line 1 to page 20, line 7:

Fig. 7 is a perspective view in a state in which the circuit substrate 30 is placed on the lower conductor plate 44. This VCO is such that a resonator and a variable capacitive element are provided in the high-frequency amplifier shown in Fig. 1B. In Fig. 7, reference numeral 61 denotes a thin-film resistor, with the termination portion of the slot 14 formed on the top surface of the circuit substrate 30 being formed into a tapered shape and this thin-film resistor 61 being provided thereon. Reference numeral 74 denotes another slot provided on the top surface of the circuit substrate 30 and, as will be described later, a slot is also provided on the back-surface side of the circuit substrate 30 with the circuit substrate 30 interposed in between, forming the planar dielectric line. Reference numeral 60 denotes a variable capacitive element mounted in such a manner as to be extended over a slot 74, whose capacitance varies according to an applied voltage. As this variable capacitive element, a variable capacitive capacitor disclosed in Japanese Unexamined Patent Publication No. 5-74655, and a conventional variable capacitive diode may be used. Reference numeral 64 in the figure denotes a section where no conductor [non-formation section for] is formed, for providing a dielectric resonator, provided on the top surface of the circuit substrate 30 and, together with the opposing conductor non-formation section for a dielectric resonator on the back-surface side of the circuit substrate 30 with this substrate interposed in between, forms a dielectric resonator of the FE010 mode in this portion. The remaining construction is the same as that of the first embodiment, and the top of the circuit substrate 30 shown in Fig. 7 is covered by an upper-part conductor plate.

Paragraph beginning at page 20, line 8 to page 21, line 21:

Fig. 8 is a plan view of the circuit substrate 30 shown in Fig. 7. Fig. 9 is a view showing the construction of the back-surface side of the circuit substrate 30. However, Fig. 9 is a view when the circuit substrate 30 is not viewed from the back-surface side, but viewed from the top surface thereof. As described above, by forming the slots 14, 24, 74, 15, 25, and 75 on both main surfaces of the circuit substrate 30 with a dielectric plate interposed therebetween, three planar dielectric lines are constructed, and further, [the conduc tor non-formation] no conductor is formed at sections 64 and 65 [for] so as to provide a dielectric resonator, [are provided] thus a dielectric resonator of the TE010 mode having a large effect of trapping an electromagnetic field is constructed in this portion. Grooves of the upper and lower conductor plates are made to oppose each other to form a space section in three mounting sections in each of the planar dielectric line, the slot line, and the FET 30, and the periphery of the section where the coplanar lines 31 and 32 are formed. In this way, a band-reflection-type oscillator is constructed. Here, in the case where the specific dielectric constant of the dielectric plate is 24 and the thickness is 0.3 mm, if the diameter of the conductor non-formation sections 64 and 65 for a dielectric resonator is set at 1.7 mm, the resonance frequency thereof can be set to 60 Ghz. Since this resonator and the planar dielectric line are not electromagnetically coupled to each other by merely bringing them close to each other, a very small cut-out section for coupling, indicated by C in [the figure] Fig. 8, is formed. A cut-out section, which is as small as the width being about 0.2 to 0.3 mm and the depth being about 0.05 to 0.1 mm, makes it possible to obtain sufficient coupling. With this construction, if the capacitance of the variable capacitive element 60 is varied, the impedance of the planar dielectric line, including the slot 74, varies, causing the resonance frequency of this planar dielectric line to vary. As a result, the resonance frequency of the dielectric resonator coupled to this line varies, making it possible to vary the oscillation frequency of the VCO.

Paragraph beginning at page 23, lines 2-9:

According to the invention [of claim 1], since the space between the planar dielectric line and the electronic components is connected via the line-conversion conductor pattern and the slot line, it is possible to perform integration by reducing the signal loss in the coupled section of the planar

dielectric line and the electronic components and while maintaining a low loss characteristic, which is a feature of the planar dielectric line.

Paragraph beginning at page 23, lines 10-21:

According to the invention [of claim 2], when the signal is propagated from one planar dielectric line of the two planar dielectric lines to the other planar dielectric line, the signal is converted into the mode of the slot line at the midpoint by the line-conversion conductor pattern and the slot line, and signal conversion is performed by the electronic components, and then the signal is returned to the mode of the planar dielectric line via the line-conversion conductor pattern. Therefore, signal conversion using electronic components is made possible with a construction with a small energy conversion loss while performing the propagation of a signal using the planar dielectric line.

Paragraph beginning at page 23, line 22 to page 24, line 4:

According to the invention [of claim 3], impedance matching is obtained between the line-conversion conductor pattern and the electronic components, and the loss in the connection section of the slot line and the electronic components is reduced.

Paragraph beginning at page 24, lines 5-9:

According to the invention [of claim 4], impedance matching is obtained between the line-conversion conductor pattern and the planar dielectric line, and the slot line, thereby suppressing unwanted reflection and reducing the transmission loss caused by line conversion.